ABSTRACT

A novel sequence of process steps is provided for forming void-free interlevel dielectric layers between closely spaced gate electrodes. Closely spaced gate electrodes having sidewall spacers are formed on a substrate. After using the sidewall spacers to form self-aligned source/drain contacts and self-aligned silicide contacts, the sidewall spacers are removed. By removing the sidewall spacers, the aspect ratio of the gap between adjacent closely spaced gate electrodes is substantially reduced (from greater than 5 to less than 2), thereby preventing voids during the subsequent deposition of an ILD layer.